IN THE CLAIMS:

Please amend claims 14 and 18 to correct a minor error as follows:

1. (Original) A receiver circuit, comprising:

a synchronous circuit that recovers and outputs a clock signal having a frequency of f1/n Hz (n: 2 or larger natural number) synchronized with input one data signal the data rate of which is f1 b/s (f1: positive real number);

"j" pieces of multipliers that output each clock signal acquired by multiplying a clock signal output from the synchronous circuit by predetermined multiple ratio via "j" pieces of interconnects (j: one or larger natural number); and

a synchronous digital circuit that has "j" pieces of parallel input terminals including one common to the input of the synchronous circuit, "j x k" pieces of parallel output terminals and "j" pieces of parallel clock input terminals, decides and recovers "j" pieces of data signals the data rate of each of which is f1 b/s and which are input to the "j" pieces of parallel input terminals using the "j" pieces of multiplied clock signals applied to the "j" pieces of parallel clock input terminals via (j + 1)th to (2 x j)th interconnects as a criterion of timing, demultiplexes the data in the ratio of "1 : k" and converts to "j x k" pieces of data signals the data rate of each of which is f1/k b/s, wherein:

the "j" pieces of parallel terminals to which data signals are input of the synchronous digital circuit function as the input terminal of the receiver circuit and the "j x k" pieces of parallel terminals from which the data signals are output function as the output terminal of the receiver circuit; and

first to "j"th interconnects connecting the output terminal of the synchronous circuit and the input terminals of the "j" pieces of multipliers and "j + 1"th to "2 x j"th interconnects connecting the "j" pieces of multipliers and the "j" pieces of parallel clock input terminals of the digital circuit are arranged so that delays t2max are smaller out of the maximum value t1max s of delays caused on the first to the "j"th interconnects and the maximum value t2max s of delays caused on the "j + 1"th to the "2 x j"th interconnects and the delays t2max are equivalent to 1/10 or less of a clock cycle 1/f1 s output from each multiplier.

2. (Original) A transmitter circuit, comprising:

a synchronous circuit to which a clock signal having a frequency of f1/m/n Hz (f1: positive real number, m: one or larger natural number, n: 2 or larger natural number) is input and from which a clock signal having a frequency of f1/n Hz and synchronized with the input clock signal is output;

"j" pieces of multipliers to which the clock signals output from the synchronous circuit are input via first to "j"th (j: one or larger natural number) interconnects and from each of which a clock signal multiplied by predetermined multiple ratio is output; and

a synchronous digital circuit that has input terminals for receiving "j x k" pieces of parallel data signals (k: 2 or larger natural number), output terminals for outputting "j" pieces of parallel data signals and "j" pieces of parallel clock input terminals, decides and recovers "j x k" pieces of data signals which are input to the input terminals and the data rate of each of which is f1/k b/s using "j" pieces of multiplied clock signals applied to "j" pieces of parallel clock input terminals via "j + 1"th to "2 x j"th interconnects as a criterion of timing, performs time-division multiplexing in the ratio of "k : 1" and converts to "j" pieces of data signals the data rate of each of which is f1 b/s, wherein:

the terminals for receiving "j x k" pieces of parallel data signals of the synchronous digital circuit function as the input terminals of the transmitter circuit and the terminals for outputting "j" pieces of parallel data output signals function as the output terminals of the transmitter circuit; and

first to "j"th interconnects connecting the output terminal of the synchronous circuit and the input terminals of "j" pieces of multipliers and "j + 1"th to "2 x j"th interconnects connecting the "j" pieces of multipliers and "j" pieces of parallel clock input terminals of the digital circuit are arranged so that delays t2max are smaller out of the maximum value t1max s of delays caused on the first to the "j"th interconnects and the maximum value t2max s of delays caused on the "j + 1"th to the "2 x j"th interconnects and the delays t2max are equivalent to 1/10 or less of a clock cycle 1/f1 s output from each multiplier.

3. (Original) The receiver circuit according to Claim 1, wherein:

the synchronous digital circuit comprises:

"j" pieces of flip-flops to which one data signal the data rate of which is f1 b/s and one clock signal having a frequency of f1 Hz are input and from which the data signal decided and recovered using the clock signal as a criterion of timing is output;

one or more frequency dividers to which the clock signal is input and from which a clock signal having a frequency equivalent to predetermined division ratio is output; and

"j" pieces of demultiplexers to which the data signal output from the flip-flop and the clock signal output from the frequency divider are input and from which "k" channels of parallel data signals the data rate of each of which is f1/k b/s (k: 2 or larger natural number) acquired by demultiplexing the time-division multiplexed data signal using the clock signal output from the frequency divider as a criterion of timing are output.

4. (Original) The transmitter circuit according to Claim 2, wherein:

the synchronous digital circuit comprises:

one or more frequency dividers to which a clock signal having a frequency of f1 Hz is input and from which a clock signal having a frequency equivalent to predetermined division ratio is output;

"j" pieces of multiplexers that time-division multiplex "k" channels of parallel data signals (k: 2 or larger natural number) the data rate of each of which is f1/k b/s and output a serial signal the data rate of which is f1 b/s; and

"j" pieces of flip-flops to each of which one data signal output from the multiplexer and one clock signal having a frequency of f1 Hz are input and from each of which the data signal decided and recovered using the clock signal as a criterion of timing is output.

5. (Original) The receiver circuit according to Claim 1, wherein:

the synchronous circuit comprises:

a voltage controlled oscillator which is provided with an input terminal that can control a frequency by an input signal and from which a clock signal having a predetermined frequency is output;

a control circuit to which a phase difference signal or a frequency difference signal is input and from which a control signal over the voltage controlled oscillator is

output; and

a phase/frequency comparator to which a data signal the data rata of which is f1 b/s and a clock signal output from the voltage controlled oscillator are input and from which a signal showing phase difference or frequency difference between the data signal and the clock signal is output, wherein:

a terminal to which a data signal is input of the phase/frequency comparator functions as the input terminal and the output terminal of the voltage controlled oscillator functions as the output terminal; and wherein:

such control that the phase of an input data signal and the phase of an output clock signal are coincident and the ratio of the data rate of f1 b/s and a frequency of f1/n Hz is fixed to predetermined ratio is made.

6. (Original) The receiver circuit according to Claim 3, wherein:

the synchronous circuit comprises:

a voltage controlled oscillator which is provided with an input terminal that can control a frequency by an input signal and from which a clock signal having a predetermined frequency is output;

a control circuit to which a phase difference signal or a frequency difference signal is input and from which a control signal over the voltage controlled oscillator is output; and

a phase/frequency comparator to which a data signal the data rate of which is f1 b/s and a clock signal output from the voltage controlled oscillator are input and from which a signal showing phase difference or frequency difference between the data signal and the clock signal is output, wherein:

a terminal to which a data signal is input of the phase/frequency comparator functions as the input terminal and the output terminal of the voltage controlled oscillator functions as the output terminal; and wherein:

such control that the phase of an input data signal and the phase of an output clock signal are coincident and the ratio of the data rate of f1 b/s and a frequency of f1/n Hz is fixed to predetermined ratio is made.

7. (Original) The transmitter circuit according to Claim 2, wherein:

the synchronous digital circuit comprises:

an input terminal to which a clock signal having a frequency of fl/n Hz is input; and

an output terminal from which a clock signal of fl/m/n Hz acquired by dividing the frequency of the clock signal in "m" pieces is output, wherein:

the synchronous circuit comprises:

an input terminal that can control a frequency by an input signal;

a voltage controlled oscillator from which a clock signal having a predetermined frequency is output;

a control circuit to which a phase difference signal or a frequency difference signal is input and from which a control signal over the voltage controlled oscillator is output; and

a phase/frequency comparator to which an input clock signal having a frequency of fl/m/n Hz and an output clock signal the frequency of which is divided output from the synchronous digital circuit are input and from which a signal showing phase difference or frequency difference between the input clock signal and the clock signal the frequency of which is divided is output; and wherein:

the synchronous circuit is controlled so that a terminal to which an input clock signal is input of the phase/frequency comparator functions as the input terminal, the output terminal of the voltage controlled oscillator functions as the output terminal, phase difference and frequency difference between the input clock signal and the clock signal the frequency of which is divided output from the synchronous digital circuit are coincident and the frequency of an output clock signal is fixed to fl/n Hz.

8. (Original) The transmitter circuit according to Claim 4, wherein:

the synchronous digital circuit comprises:

an input terminal to which a clock signal having a frequency of fl/n Hz is input; and

an output terminal from which a clock signal having a frequency of fl/m/n Hz acquired by dividing the frequency of the clock signal in "m" pieces is output, wherein:

the synchronous circuit comprises:

an input terminal that can control a frequency by an input signal;

a voltage controlled oscillator from which a clock signal having a

predetermined frequency is output;

a control circuit to which a phase difference signal or a frequency difference signal is input and from which a control signal over the voltage controlled oscillator is output; and

a phase/frequency comparator to which an input clock signal having a frequency of fl/m/n Hz and an output clock signal the frequency of which is divided output from the synchronous digital circuit are input and from which a signal showing phase difference or frequency difference between the input clock signal and the clock signal the frequency of which is divided is output; and wherein:

the synchronous circuit is controlled so that a terminal to which an input clock signal is input of the phase/frequency comparator functions as the input terminal, the output terminal of the voltage controlled oscillator functions as the output terminal, phase difference and frequency difference between the input clock signal and the clock signal the frequency of which is divided output from the synchronous digital circuit are coincident and the frequency of an output clock signal is fixed to fl/n Hz.

9. (Original) The receiver circuit according to Claim 1, further comprising:

a photo diode that converts an optical signal to an electrical signal; and

a preamplifier that amplifies a signal from the photo diode, wherein:

the data signal input to the receiver circuit is an optical signal;

the optical signal is converted to an electrical signal via the photo diode and is input to the preamplifier; and

the output of the preamplifier is input to the synchronous digital circuit as a data input signal.

10. (Original) The receiver circuit according to Claim 3, further comprising:

a photo diode that converts an optical signal to an electrical signal; and

a preamplifier that amplifies a signal from the photo diode, wherein:

the data signal input to the receiver circuit is an optical signal;

the optical signal is converted to an electrical signal via the photo diode and is input to the preamplifier; and

the output of the preamplifier is input to the synchronous digital circuit as a data input signal.

11. (Original) The receiver circuit according to Claim 5, further comprising:

a photo diode that converts an optical signal to an electrical signal; and

a preamplifier that amplifies a signal from the photo diode, wherein:

the data signal input to the receiver circuit is an optical signal;

the optical signal is converted to an electrical signal via the photo diode and is input to the preamplifier; and

the output of the preamplifier is input to the synchronous digital circuit as a data input signal.

12. (Original) The transmitter circuit according to Claim 2, further comprising:

a driver that amplifies a data signal output from the synchronous digital circuit;

a laser oscillator that generates an optical signal; and

a modulator that outputs a modulated signal acquired by modulating the optical signal according to a modulating signal output from the driver, wherein:

the driver, the laser oscillator and the modulator are provided between the output terminal of the synchronous digital circuit and the output terminal of the transmitter circuit; and

a data signal output from the output terminal of the transmitter circuit is an optical signal.

13. (Original) The transmitter circuit according to Claim 4, further comprising:

a driver that amplifies a data signal output from the synchronous digital circuit;

a laser oscillator that generates an optical signal; and

a modulator that outputs a modulated signal acquired by modulating the optical signal according to a modulating signal output from the driver, wherein:

the driver, the laser oscillator and the modulator are provided between the output terminal of the synchronous digital circuit and the output terminal of the transmitter circuit; and

a data signal output from the output terminal of the transmitter circuit is an optical signal.

14. (Currently Amended) The ~~transmitter~~ receiver circuit according to Claim 6, further comprising:

a driver that amplifies a data signal output from the synchronous digital circuit;

a laser oscillator that generates an optical signal; and

a modulator that outputs a modulated signal acquired by modulating the optical signal according to a modulating signal output from the driver, wherein:

the driver, the laser oscillator and the modulator are provided between the output terminal of the synchronous digital circuit and the output terminal of the transmitter circuit; and

a data signal output from the output terminal of the transmitter circuit is an optical signal.

15. (Original) The receiver circuit according to Claim 1, wherein:

the multiplier includes an exclusive-OR circuit and a 90-degree phase shifter; and

a signal input to the multiplier is branched, one is input to the exclusive-OR circuit, the branched other signal is input to the other terminal of the exclusive-OR circuit via the 90-degree phase shifter and the output of the exclusive-OR circuit functions as the output of the multiplier.

16. (Original) The receiver circuit according to Claim 3, wherein:

the multiplier includes an exclusive-OR circuit and a 90-degree phase shifter; and

a signal input to the multiplier is branched, one is input to the exclusive-OR circuit, the branched other signal is input to the other terminal of the exclusive-OR circuit via the 90-degree phase shifter and the output of the exclusive-OR circuit functions as the output of the multiplier.

17. (Original) The receiver circuit according to Claim 5, wherein:

the multiplier includes an exclusive-OR circuit and a 90-degree phase shifter; and

a signal input to the multiplier is branched, one is input to the exclusive-OR circuit, the branched other signal is input to the other terminal of the exclusive-OR circuit via the 90-degree phase shifter and the output of the exclusive-OR circuit functions as the output of the multiplier.

18. (Currently Amended) The ~~receiver~~ transmitter circuit according to Claim 7, wherein:

the multiplier includes an exclusive-OR circuit and a 90-degree phase shifter; and

a signal input to the multiplier is branched, one is input to the exclusive-OR circuit, the branched other signal is input to the other terminal of the exclusive-OR circuit via the 90-degree phase shifter and the output of the exclusive-OR circuit functions as the output of the multiplier.

19. (Original) A transceiver circuit comprising a receiver circuit and a transmitter circuit, wherein:

the receiver circuit comprises:

a synchronous circuit that recovers and outputs a clock signal having a frequency of f1/n Hz (n: 2 or larger natural number) synchronized with input one data signal the data rate of which is f1 b/s (f1: positive real number);

"j" pieces of multipliers that output each clock signal acquired by multiplying a clock signal output from the synchronous circuit by predetermined multiple ratio via "j" pieces of interconnects (j: one or larger natural number); and

a synchronous digital circuit that has "j" pieces of parallel input terminals including one common to the input of the synchronous circuit, "j x k" pieces of parallel output terminals and "j" pieces of parallel clock input terminals, decides and recovers "j" pieces of data signals the data rate of each of which is f1 b/s and which are input to the "j" pieces of parallel input terminals using the "j" pieces of multiplied clock signals applied to the "j" pieces of parallel clock input terminals via (j + 1)th to (2 x j)th interconnects as a criterion of timing, demultiplexes the data in the ratio of "1 : k" and converts to "j x k" pieces of data signals the data rate of each of which is f1/k b/s, wherein:

the "j" pieces of parallel terminals to which data signals are input of the synchronous digital circuit function as the input terminal of the receiver circuit and

the "j x k" pieces of parallel terminals from which the data signals are output function as the output terminal of the receiver circuit; and

first to "j"th interconnects connecting the output terminal of the synchronous circuit and the input terminals of the "j" pieces of multipliers and "j + 1"th to "2 x j"th interconnects connecting the "j" pieces of multipliers and the "j" pieces of parallel clock input terminals of the digital circuit are arranged so that delays t2max are smaller out of the maximum value t1max s of delays caused on the first to the "j"th interconnects and the maximum value t2max s of delays caused on the "j + 1"th to the "2 x j"th interconnects and the delays t2max are equivalent to 1/10 or less of a clock cycle 1/f1 s output from each multiplier, wherein:

the transmitter circuit comprises:

a synchronous circuit to which a clock signal having a frequency of f1/m/n Hz (f1: positive real number, m: one or larger natural number, n: 2 or larger natural number) is input and from which a clock signal having a frequency of f1/n Hz and synchronized with the input clock signal is output;

"j" pieces of multipliers to which the clock signals output from the synchronous circuit are input via first to "j"th (j: one or larger natural number) interconnects and from each of which a clock signal multiplied by predetermined multiple ratio is output; and

a synchronous digital circuit that has input terminals for receiving "j x k" pieces of parallel data signals (k: 2 or larger natural number), output terminals for outputting "j" pieces of parallel data signals and "j" pieces of parallel clock input terminals, decides and recovers "j x k" pieces of data signals which are input to the input terminals and the data rate of each of which is f1/k b/s using "j" pieces of multiplied clock signals applied to "j" pieces of parallel clock input terminals via "j + 1"th to "2 x j"th interconnects as a criterion of timing, performs time-division multiplexing in the ratio of "k : 1" and converts to "j" pieces of data signals the data rate of each of which is f1 b/s, wherein:

the terminals for receiving "j x k" pieces of parallel data signals of the synchronous digital circuit function as the input terminals of the transmitter circuit and the terminals for outputting "j" pieces of parallel data output signals function as the output terminals of the transmitter circuit; and

first to "j"th interconnects connecting the output terminal of the synchronous

circuit and the input terminals of "j" pieces of multipliers and "j + 1"th to "2 x j"th interconnects connecting the "j" pieces of multipliers and "j" pieces of parallel clock input terminals of the digital circuit are arranged so that delays t2max are smaller out of the maximum value t1max s of delays caused on the first to the "j"th interconnects and the maximum value t2max s of delays caused on the "j + 1"th to the "2 x j"th interconnects and the delays t2max are equivalent to 1/10 or less of a clock cycle 1/f1 s output from each multiplier.